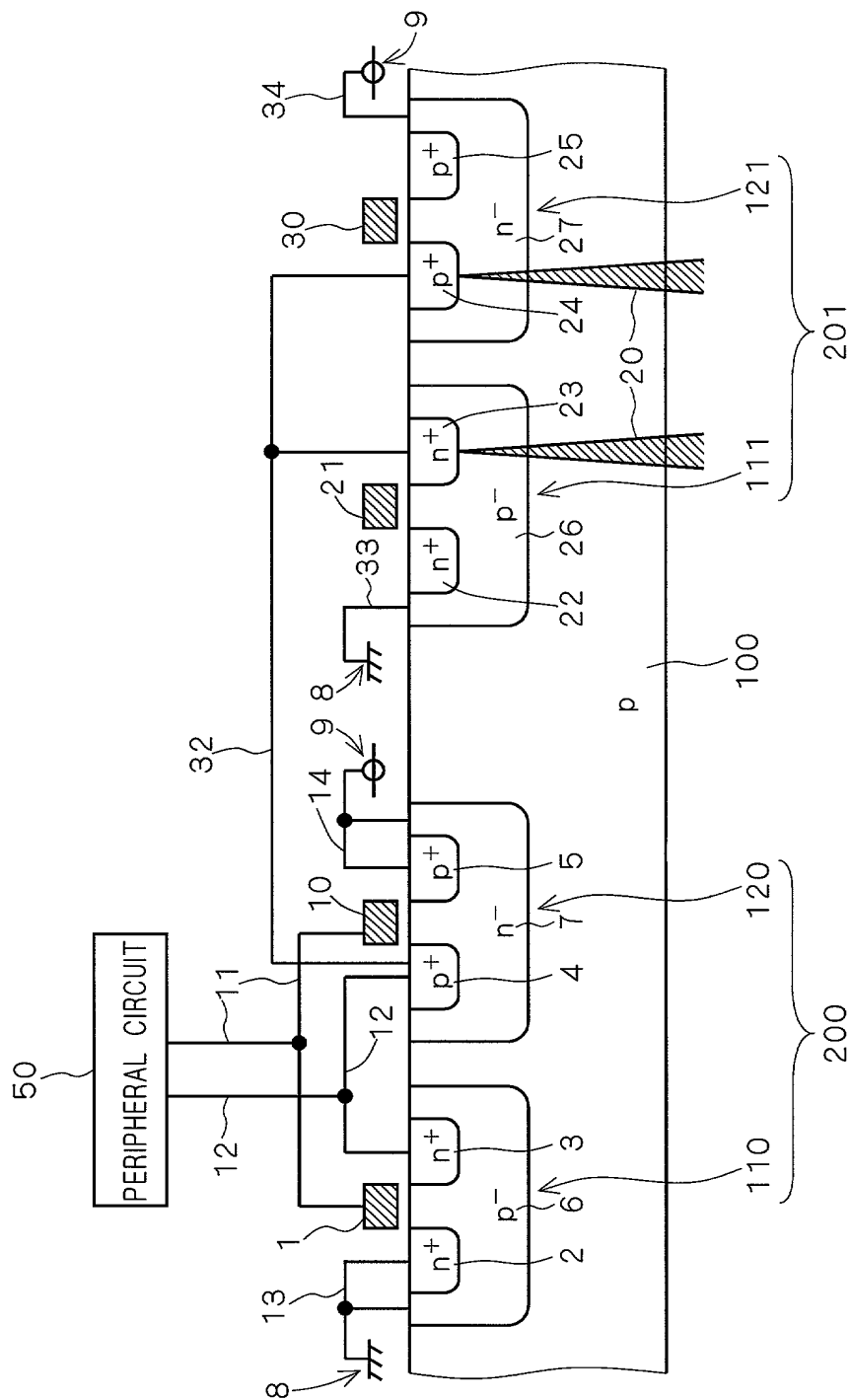


This diagram shows a cross-sectional view of a semiconductor device. A substrate 100 is divided into a peripheral circuit region 120 and a main circuit region 200. The peripheral circuit region 120 includes a peripheral circuit 50, which is connected to a gate electrode 11 and a gate electrode 12. The main circuit region 200 includes a main circuit 100, which is connected to a gate electrode 13 and a gate electrode 14. The main circuit 100 is further divided into a first main circuit 110 and a second main circuit 121. The first main circuit 110 includes a gate electrode 111 and a gate electrode 112. The second main circuit 121 includes a gate electrode 121 and a gate electrode 122. The main circuit 100 is also connected to a gate electrode 13 and a gate electrode 14. The main circuit 100 is further divided into a first main circuit 110 and a second main circuit 121. The first main circuit 110 includes a gate electrode 111 and a gate electrode 112. The second main circuit 121 includes a gate electrode 121 and a gate electrode 122. The main circuit 100 is also connected to a gate electrode 13 and a gate electrode 14. The main circuit 100 is further divided into a first main circuit 110 and a second main circuit 121. The first main circuit 110 includes a gate electrode 111 and a gate electrode 112. The second main circuit 121 includes a gate electrode 121 and a gate electrode 122. The main circuit 100 is also connected to a gate electrode 13 and a gate electrode 14.

F / G. 2



F/G. 3

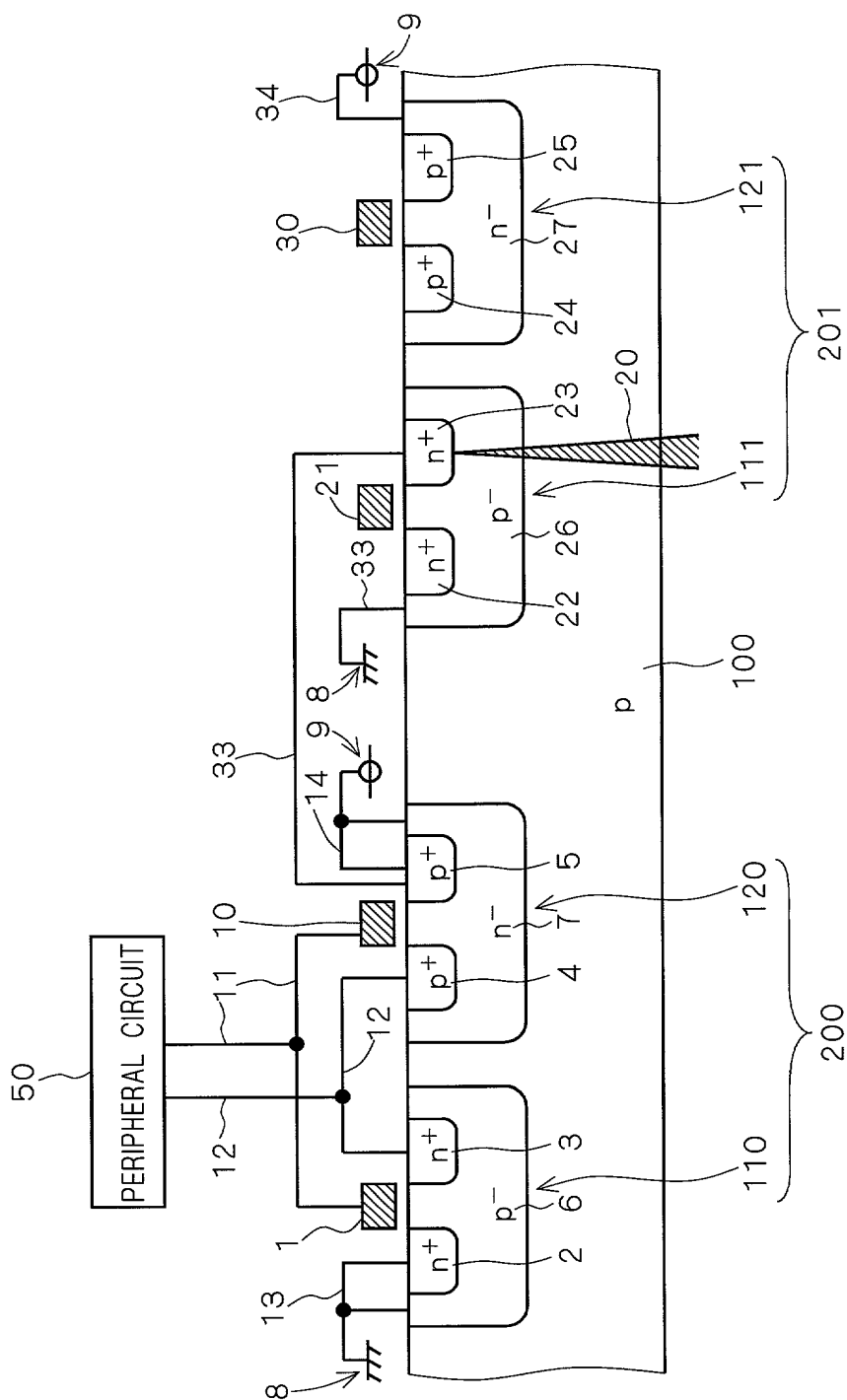
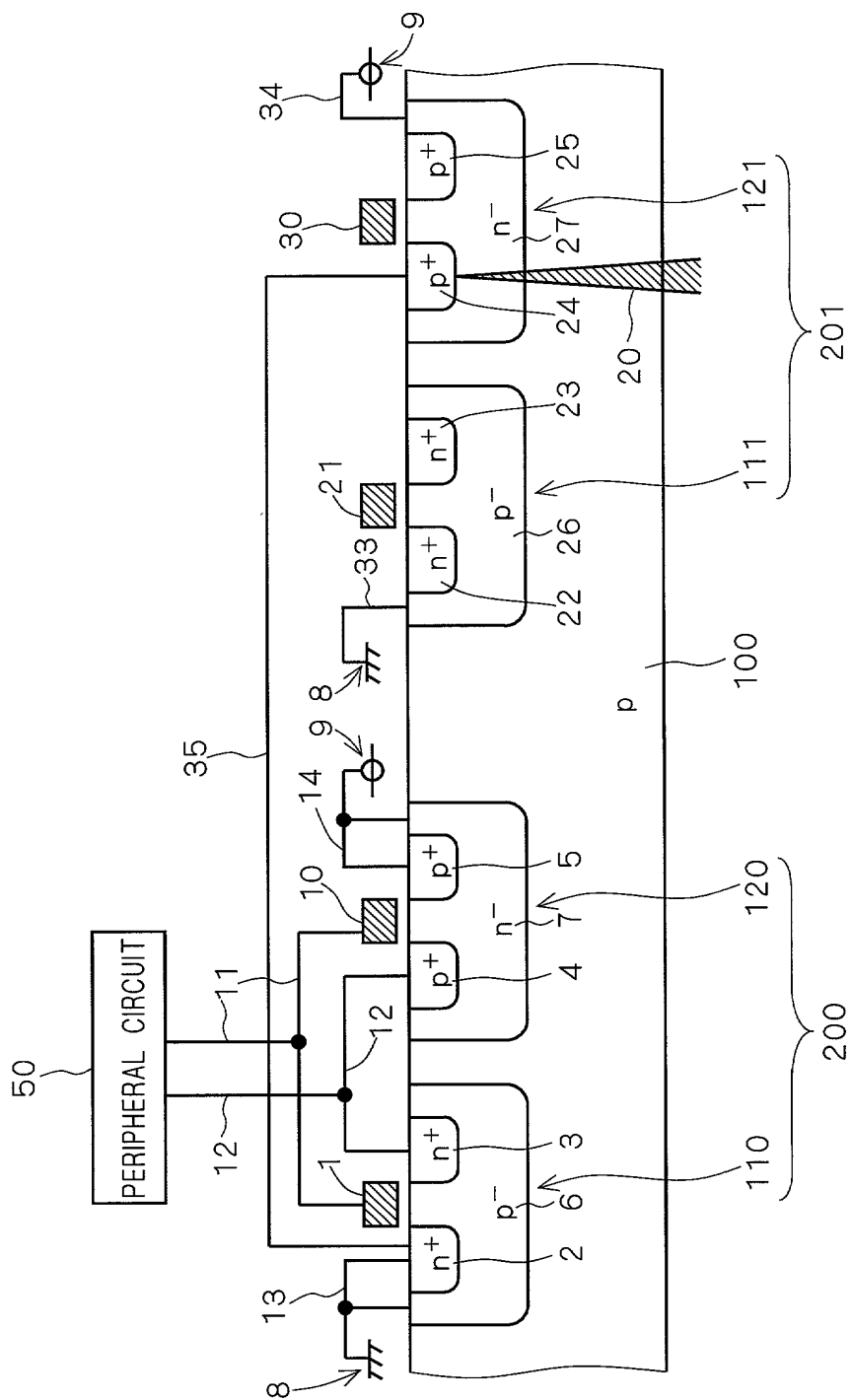


FIG. 4



This diagram shows a cross-sectional view of a semiconductor device. A substrate 100 is divided into a peripheral circuit region 200 and a main circuit region 201. The peripheral circuit region 200 contains a peripheral circuit 50, which includes a gate stack 8, a source/drain region 13, and a gate stack 14. The main circuit region 201 contains a main circuit 10, which includes a gate stack 21, a source/drain region 22, and a gate stack 23. The device is formed on a p-type substrate 100. The peripheral circuit region 200 includes a p+ region 4, an n+ region 5, and a p- region 6. The main circuit region 201 includes a p+ region 7, an n+ region 8, and a p- region 9. The device is formed on a p-type substrate 100. The peripheral circuit region 200 includes a p+ region 4, an n+ region 5, and a p- region 6. The main circuit region 201 includes a p+ region 7, an n+ region 8, and a p- region 9.

FIG. 6

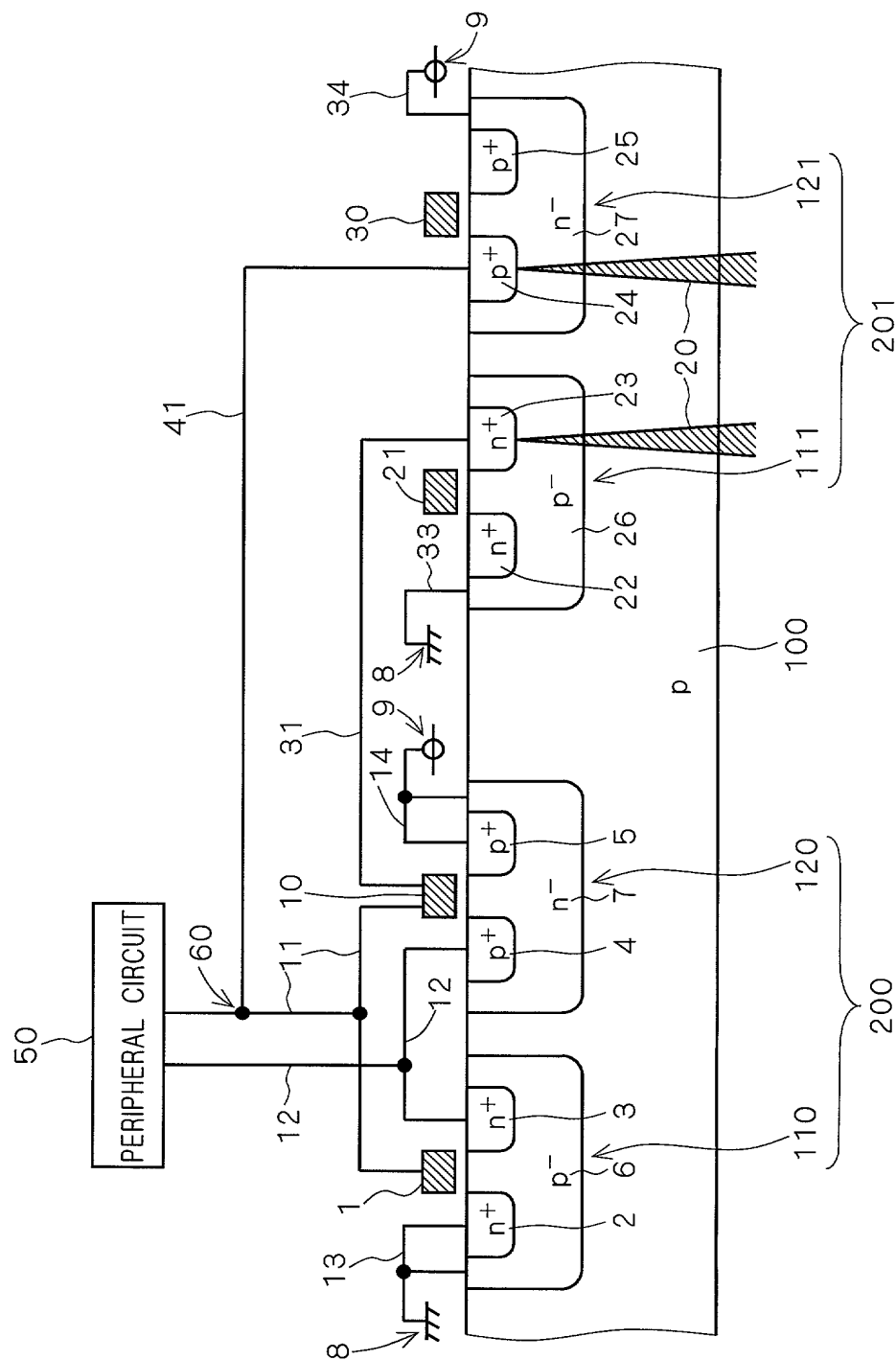


FIG. 7

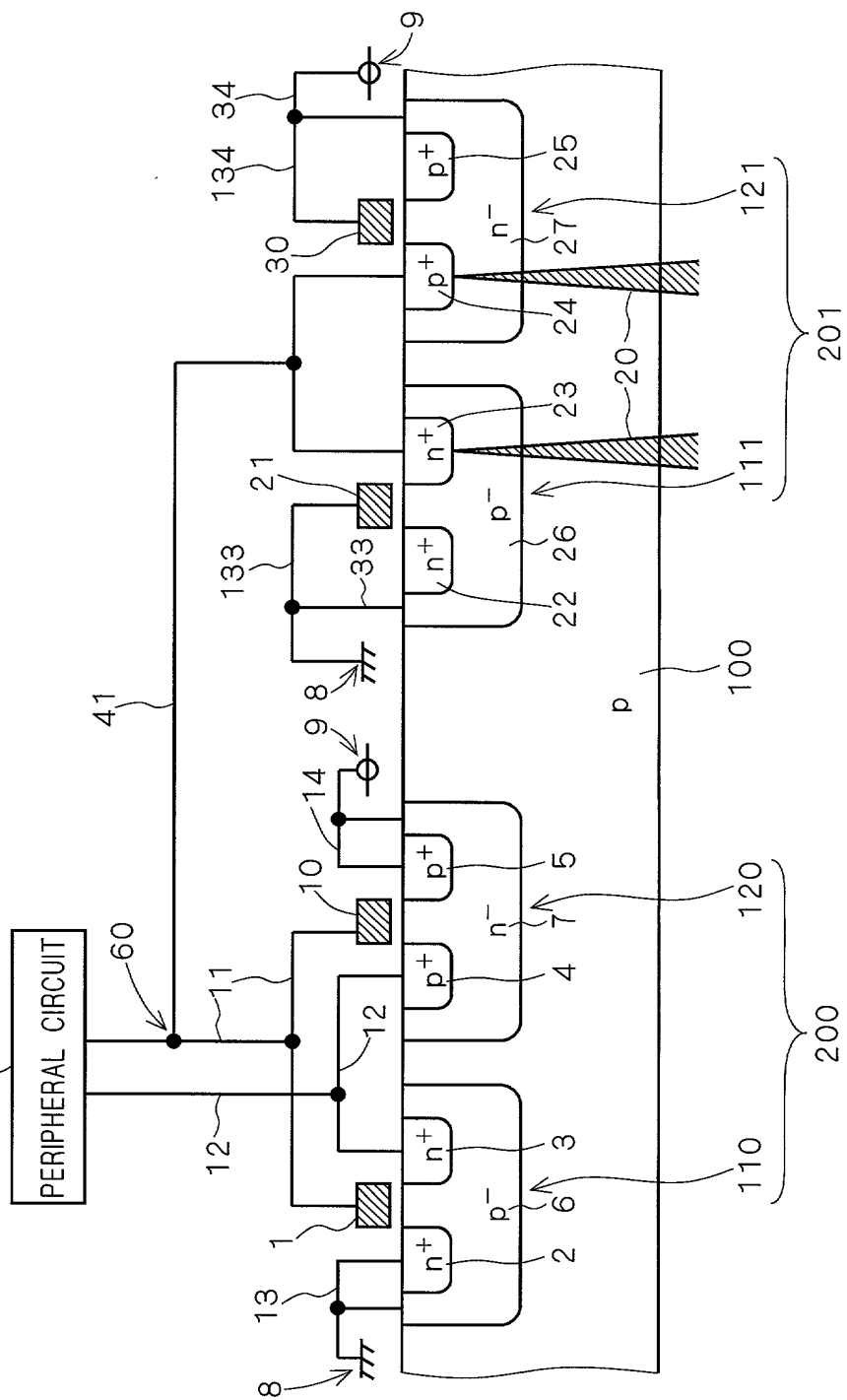


FIG. 8

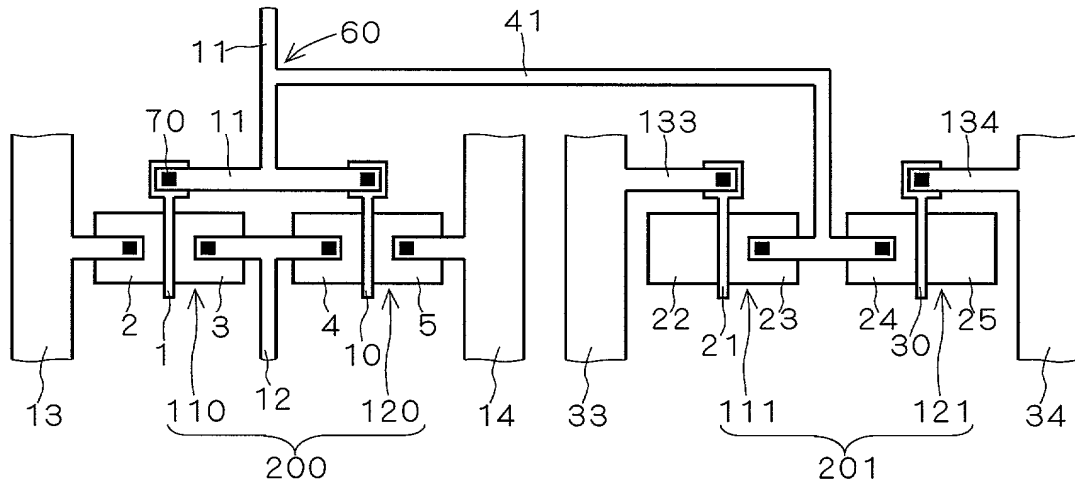


FIG. 9A

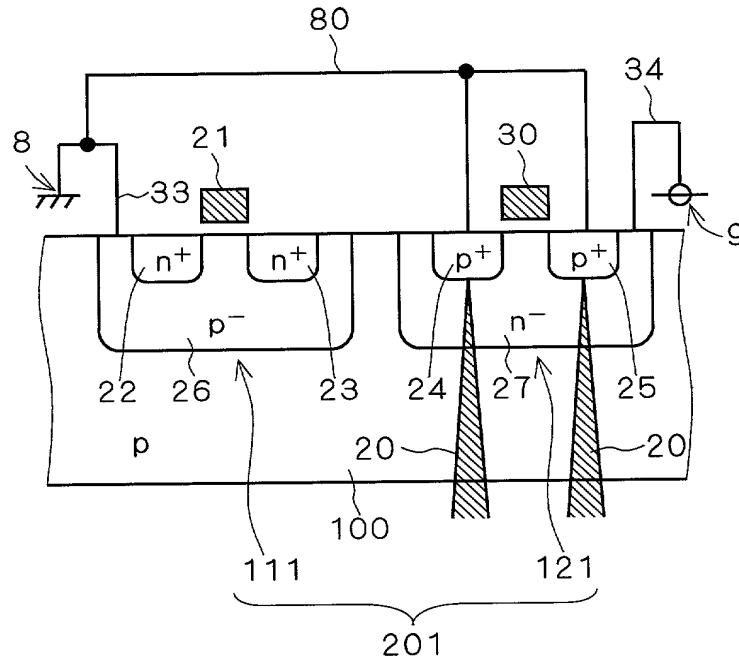


FIG. 9B

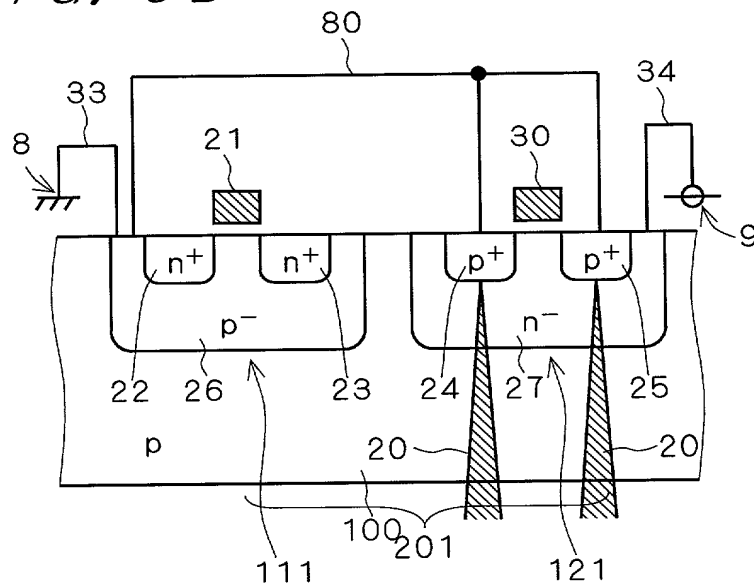


FIG. 10A

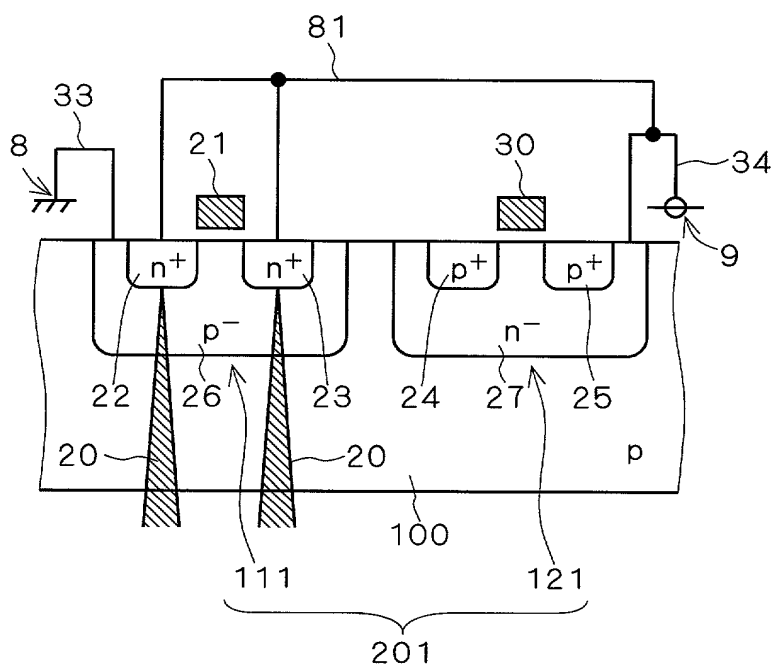
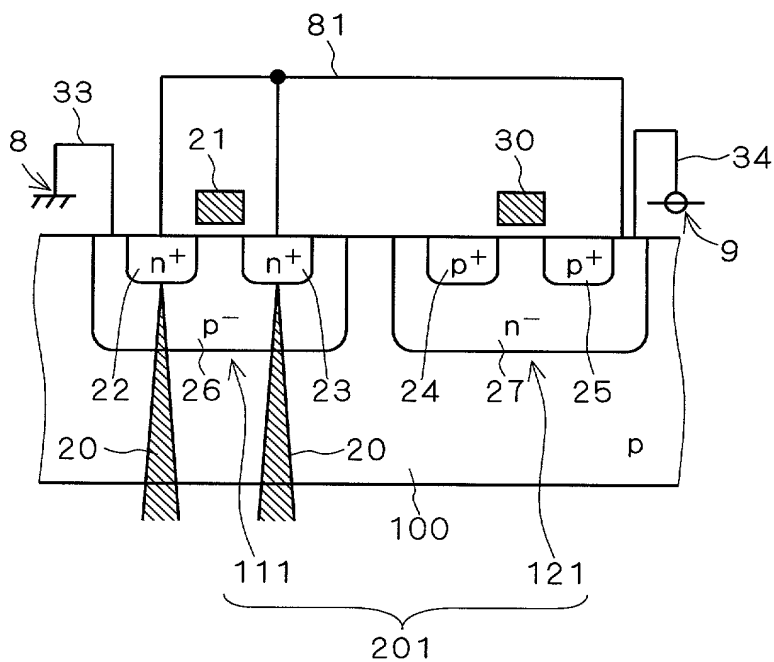


FIG. 10B



$$F/G. \quad 11$$
